

REMARKS

By this Preliminary Amendment, Applicant AMENDS the specification, the title of the invention and the abstract of the disclosure.

Applicant has attached hereto a Substitute Specification in order to make corrections of minor informalities contained in the originally filed specification. Applicant's undersigned representative hereby declares and states that the Substitute Specification filed concurrently herewith does not add any new matter whatsoever to the above-identified patent application. Accordingly, entry and consideration of the Substitute Specification are respectfully requested.

The changes to the specification have been made to correct minor informalities to facilitate examination of the present application.

Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are respectfully solicited.

Respectfully submitted,

Date: March 21, 2006

/Joseph R. Keating #37,368/

Attorney for Applicant(s)

Joseph R. Keating
Registration No. 37,368

KEATING & BENNETT, LLP
8180 Greensboro Drive, Suite 850
Tyson's Corner, Virginia 22102
Telephone: (703) 637-1480
Facsimile: (703) 637-1499

10/572730

IAP20 Rec'd PCT/PTO 21 MAR 2006

MARKED-UP VERSION OF
ENGLISH TRANSLATION OF
INTERNATIONAL APPLICATION
AS ORIGINALLY FILED

JAP20 Rec'd PCT/PTO 21 MAR 2006

~~DESCRIPTION~~

Attorney Docket Number: 70404.30/tt

5 SEMICONDUCTOR DEVICE HAVING HIGH-K GATE DIELECTRIC LAYER
AND METHOD FOR MANUFACTURING THE SAME

~~Technical Field~~

[0001]

10 1. Field of the Invention

The present invention relates to a semiconductor device having a high-k gate dielectric layer and a method for manufacturing the ~~same~~-semiconductor device. More particularly, the present invention relates to the control of the threshold voltage of a MISFET.

15

~~Background Art~~

[0002]

2. Description of the Background Art

In order to realize a high-speed performance and ~~scale-down~~size
20 reduction of semiconductor devices, such as a MISFET (metal insulator
semiconductor field effect transistor), a thin gate dielectric layer
has been adopted. However, a problem that gate leakage current
increases ~~occurred~~ when the thickness of a silicon oxide film and
a silicon oxynitride film (hereinafter referred to as "a silicon oxide
25 film and the like") is reduced. The silicon oxide film and the like
have ~~hitherto~~ been used as gate dielectric layers. To solve this
problem, there has been proposed a technique which involves adopting
a film having high dielectric constant (k) (hereinafter referred to
as "a high-k gate dielectric layer") as a gate dielectric layer.

30 [0003]

Also, there has been proposed a technique which involves controlling the threshold voltage of a MOS (metal oxide semiconductor)

transistor by forming P-type impurity regions (refer to, for example,
Japanese Patent Document 1 Laid-Open No. 2002-313950).

[0004]

~~{Patent Document 1}~~

5 ~~Japanese Patent Laid Open No. 2002-313950~~

~~Disclosure~~ However, as a result of an examination by the ~~Invention~~

~~Objectives which~~ present inventor, it became apparent that the
~~Invention solves~~ use of a high-k gate dielectric layer as a gate
10 ~~dielectric layer of a MISFET causes the problem that the threshold~~
~~voltage of a MISFET rises more than when a silicon oxide film and~~
~~the like are used. As one cause, it might be that this is because~~
~~the metals contained in a high-k gate dielectric layer and the Si~~
~~contained in a gate electrode react with each other. Furthermore,~~
15 ~~as another cause it might be that this is because the metals contained~~
~~in a high-k gate dielectric layer react with arsenic ions and boron~~
~~ions implanted into a substrate for use in the formation of source/drain~~
~~regions.~~

[0005]

20 ~~However, as a result of an examination by the present inventor,~~
~~it became apparent that the use of a high k gate dielectric layer~~
~~as a gate dielectric layer of a MISFET arises the problem that the~~
~~threshold voltage of a MISFET further rises compared to a case where~~
~~a silicon oxide film and the like are used. As one cause, it might~~
25 ~~be thought that this is because the metals contained in a high k gate~~
~~dielectric layer and the Si contained in a gate electrode react with~~
~~each other. Furthermore, as another cause, it might be thought that~~
~~this is because the metals contained in a high k gate dielectric layer~~
~~react with arsenic ions and boron ions implanted into a substrate~~
30 ~~for use in the formation of source/drain regions.~~

~~{0006}~~

Since the driving performance of a transistor decreases if the threshold voltage of a MISFET rises, it is necessary to control the threshold voltage with high accuracy.

5

SUMMARY OF THE INVENTION

[0006]

The present invention has been conceived to solve the problems described above and preferred embodiments of the present invention provide a novel and useful semiconductor device and method for
10 manufacturing the same, so as to control a threshold voltage of the semiconductor device having a high-k gate dielectric layer with high accuracy.

[0007]

~~The present invention has been conceived to solve the~~
15 ~~previously mentioned problems and an object of the present invention is to control a threshold voltage of a semiconductor device having a high-k gate dielectric layer with high accuracy.~~

~~Means to solve the Objectives~~

20 According to first aspect of the present invention, the semiconductor device according to a preferred embodiment includes a well of a first conductive type formed in an upper layer of a substrate. A low-concentration layer of the first conductive type having a lower impurity concentration than the well is formed in an extreme surface
25 layer of a channel portion of the well. A high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film is formed on the low-concentration layer. A gate electrode is formed on the high-k gate dielectric layer. Source/drain regions of a second conductive type are formed in an upper layer of the well, the
30 source/drain regions sandwiching the low-concentration layer.

[0008]

According to ~~first-second~~ aspect of the present invention, the complementary semiconductor device ~~comprises a well of a first~~

~~conductive having a n-type circuit region and a p-type circuit region,~~
~~includes a p-type well formed in an upper layer of a substrate.—A~~
~~low concentration layer of the first conductive type having a lower~~
~~impurity concentration than the well is formed in an n-type circuit~~
5 ~~region. A n-type well is formed in an upper layer of the substrate~~
~~of the p-type circuit region. A p-type low-concentration layer is~~
~~formed in an extreme surface layer of a channel portion of the p-type~~
~~well. A high k gate dielectric layer having a higher dielectric~~
~~constant than a silicon oxide film is formed on, the p-type~~
10 ~~low-concentration layer. A gate electrode is formed on the high k~~
~~gate dielectric layer. Source/drain regions of a second conductive~~
~~type are formed in an upper layer of the having a lower impurity~~
~~concentration than the p-type well.~~ An n-type low-concentration
layer is formed in an extreme surface layer of a channel portion of
15 the n-type well, the n-type low-concentration having a lower impurity
concentration than the n-type well. A high-k gate dielectric layer
is formed on the p-type and n-type low-concentration layers, the high-k
gate dielectric layer having a higher dielectric constant than a
silicon oxide film. A gate electrode is formed on the high-k gate
20 dielectric layer. N-type source/drain regions are formed in an upper
layer of the p-type well, the n-type source/drain regions sandwiching
the p-type low-concentration layer. P-type source/drain regions
are formed in an upper layer of the n-type well, the p-type source/drain
regions sandwiching the n-type low-concentration layer.

25 [0009]

According to ~~second~~ third aspect of the present invention, in
the ~~complementary method for manufacturing a semiconductor device~~
~~having a n-type circuit region and~~ according to another preferred
embodiment of the present invention, a p-type circuit region, comprises
30 a p-type well is firstly formed in an upper layer of by implanting
a first conductive type impurity into a substrate of the n-type circuit
region. A n-type well is formed in an upper layer of the substrate
of the p-type circuit region. A p-type low concentration layer second

conductive type impurity is formed in~~implanted into an extreme surface layer of a channel portion of the p-type well, the p-type low concentration layer having a lower impurity concentration than the p-type well. A n-type low concentration layer is formed in an~~
5 ~~extreme surface layer of a channel portion of the n-type well, the n-type low concentration having a lower impurity concentration than the n-type well. A high-k gate dielectric layer is formed on the p-type and n-type low concentration layers, the high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film.~~
10 ~~A gate electrode is formed.~~ A high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film is formed on the substrate, after implanting the second conductive type impurity. A gate electrode material film to be a gate electrode is formed on the high-k gate dielectric layer. N-type source/drain regions are
15 ~~formed in an upper layer of the p-type well, the n-type source/drain regions sandwiching the p-type low concentration layer. P-type source/drain regions are formed in an upper layer of the n-type well, the p-type source/drain regions sandwiching the n-type low concentration layer.~~ A gate electrode is formed by patterning the
20 gate electrode material film and the high-k gate dielectric layer. Source/drain regions are formed by implanting a second conductive type impurity into the substrate by using the gate electrode as a mask.

[0010]

25 According to ~~third~~fourth aspect of the present invention, in the method for manufacturing a complementary semiconductor device, a p-type well is firstly formed by implanting a first conductive type impurity into a~~in an upper layer of a substrate. A second conductive type impurity is~~ of the n-type circuit region. An n-type well is
30 formed in the upper layer of the substrate of the p-type circuit region. N-type impurities are implanted into an extreme surface layer of a channel portion of the p-type well. P-type impurities are implanted into an extreme surface layer of a channel portion of the n-type well.

A high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film is formed on the substrate, after implanting the ~~second conductive type impurity~~ n-type and p-type impurities. A gate electrode material film to be a gate electrode is formed on
5 the high-k gate dielectric layer. A gate electrode is formed by patterning the gate electrode material film and the high-k gate dielectric layer. ~~Source~~ in the n-type and p-type circuit regions. N-type source/drain regions are formed by implanting a second
conductive the n-type impurity into the substrate p-type well by using
10 the gate electrode as a mask. P-type source/drain regions are formed
in the p-type circuit region by implanting the p-type impurity into
then-type well by using the gate electrode as a mask.

[0011]

According to ~~fourth~~ fifth aspect of the present invention, in
15 the method for manufacturing a complementary semiconductor device,
a p-type well is firstly formed in by implanting boron ions with a
dosage of 1×10^{13} atoms/cm² into an upper layer of a substrate of
in the n-type circuit region. ~~A~~ An n-type well is formed ~~in the~~ by
implanting phosphorus ions with a dosage of 1×10^{13} atoms/cm² into
20 an upper layer of the substrate of in the p-type circuit region. ~~N-type~~
~~impurities is~~ Arsenic or phosphorus ions are implanted with a dosage
of 5 to 8×10^{12} atoms/cm² into an extreme surface layer of a channel
portion of the p-type well. ~~P-type impurities is~~ Boron ions are
implanted with a dosage of 3 to 5×10^{12} atoms/cm² into an extreme
25 surface layer of a channel portion of the n-type well. ~~A high-k gate~~
~~dielectric layer having a higher dielectric constant than a silicon~~
~~oxide film is formed on the substrate, after implanting the n-type~~
~~and p-type impurities~~. ~~A gate electrode material film to be a gate~~
~~electrode is formed on the high-k gate dielectric layer~~. ~~A gate~~
30 ~~electrode is formed by patterning the gate electrode material film~~
~~and the high-k gate dielectric layer in the n-type and p-type circuit~~
~~regions~~. P-type and n-type low-concentration layers are formed on
an extreme surface layer of a channel portion of the p-type and n-type

wells by diffusing the arsenic or phosphorus and boron ions implanted into the extreme surface layer by performing a heat treatment. A HfAlOx film is formed on the substrate, after performing the heat treatment. A polycrystalline silicon film to be a gate electrode is formed on the HfAlOx film. A gate electrode is formed on the p-type and n-type low-concentration layers via the HfAlOx film by patterning the polycrystalline silicon film and HfAlOx film. N-type source/drain regions are formed by implanting the n-type impurity impurities into the p-type well by using the gate electrode as a mask. P-type source/drain regions are formed in the p-type circuit region by implanting the p-type impurity impurities into the n-type well by using the gate electrode as a mask.

[0012]

According to fifth aspect of the present invention, in the method for manufacturing a complementary semiconductor device, a p-type well is firstly formed by implanting boron ions with a dosage of 1×10^{13} atoms/cm² into an upper layer of a substrate in the n-type circuit region. A n-type well is formed by implanting phosphorus ions with a dosage of 1×10^{13} atoms/cm² into an upper layer of the substrate in the p-type circuit region. Arsenic or phosphorus ions are implanted with a dosage of 5 to 8×10^{12} atoms/cm² into an extreme surface layer of a channel portion of the p-type well. Boron ions are implanted with a dosage of 3 to 5×10^{12} atoms/cm² into an extreme surface layer of a channel portion of the n-type well. P-type and n-type low concentration layers are formed on an extreme surface layer of a channel portion of the p-type and n-type wells by diffusing the arsenic or phosphorus and boron ions implanted into the extreme surface layer by performing a heat treatment. A HfAlOx film is formed on the substrate, after performing the heat treatment. A polycrystalline silicon film to be a gate electrode is formed on the HfAlOx film. A gate electrode is formed on the p-type and n-type low concentration layers via the HfAlOx film by patterning the polycrystalline silicon film and HfAlOx film. N-type source/drain

~~regions are formed by implanting n-type impurities into the p-type well by using the gate electrode as a mask. P-type source/drain regions are formed in the p-type circuit region by implanting p-type impurities into the n-type well by using the gate electrode as a mask.~~

5

~~Effects of the Invention~~

~~According to the present invention, by forming a low concentration layer having a low impurity concentration in an extreme surface layer of a channel portion of a well region, it is possible to control the threshold voltage of a semiconductor device having a high k gate dielectric layer with high accuracy.~~

10

~~Brief Description of the Drawings~~

~~Other features, elements, steps, advantages and characteristics of the present invention will be apparent from the following detailed description of preferred embodiments of the present invention when read in conjunction with the accompanying drawings.~~

15

BRIEF DESCRIPTION OF THE DRAWINGS

20 [0013]

Fig. 1 is a sectional view for describing a semiconductor device according to a first preferred embodiment of the present invention;

[0014]

~~Fig. 1 is a sectional view for describing a semiconductor device according to a first embodiment of the present invention;~~

25

Figs. 2A to 2F are sectional process views for describing a method for manufacturing a semiconductor device according to the first preferred embodiment of the present invention;

30

~~Fig. 3 is a sectional view for describing a semiconductor device according to a second embodiment of the present invention;~~

~~Figs. 4A to 6C are sectional process views for describing a method for manufacturing a semiconductor device according to the second embodiment of the present invention;~~

~~Fig. 7 is a diagram for showing a relationship between a threshold voltage and a gate length of a n-type channel MISFET according to the present invention; and~~

~~Fig. 8 is a diagram for showing a relationship between a threshold voltage and a gate length of a p-type channel MISFET according to the present invention.~~

~~Explanation of the numerals~~

~~[0015]~~

- 10 ~~1,21 silicon substrate~~
- ~~2,22 element isolation structures~~
- ~~Fig. 3,23 p-type well~~
- ~~4,26 arsenic ions~~
- ~~5,27 p-type low concentration layer~~
- 15 ~~6,31 silicon oxide film~~
- ~~7,32 high k gate dielectric layer~~
- ~~8,33 polycrystalline silicon film~~
- ~~8a,33a gate electrode~~
- ~~9,34 resist pattern~~
- 20 ~~10,36 arsenic ions~~
- ~~11,37 n-type impurity layers~~
- ~~11a,37a n-type extension regions~~
- ~~12,41 silicon oxide film~~
- ~~13,42 sidewall spacers (silicon nitride film)~~
- 25 ~~14,44 arsenic ions~~
- ~~15,45 n-type impurity layer~~
- ~~15a,45a n-type source/drain regions~~
- ~~24 n-type well~~
- ~~25,28,35,38,43,46 resist pattern~~
- 30 ~~29 boron ions~~
- ~~39 boron ions~~
- ~~40 p-type impurity layer~~
- ~~40a p-type extension regions~~

~~47 boron ions~~

~~48 p-type impurity layers~~

~~48a p-type source/drain regions~~

5 ~~Best mode~~ is a sectional view for carrying out describing a
semiconductor device according to a second preferred embodiment of
the ~~Invention~~ present invention;
[0016]

Embodiments of the present invention will be described with
10 reference to the accompanying drawings. The portions that are common
to some of the drawings are given the same reference numerals and
redundant descriptions therefore may be omitted.

~~First Embodiment~~

Figs. 4A to 6C are sectional process views for describing a method
15 for manufacturing a semiconductor device according to the second
preferred embodiment of the present invention;
[0017]

Fig. 1 ~~is a sectional view for describing a semiconductor device~~
~~according to a first embodiment of the present invention. Concretely,~~
20 ~~Fig. 1 is a sectional view for describing a n-type channel MISFET.~~ 7
is a diagram for showing a relationship between a threshold voltage
and a gate length of a n-type channel MISFET according to various
preferred embodiments of the present invention; and
[0018]

25 ~~As shown in Fig. 1, element isolation structures 2 for isolating~~
~~active regions of a silicon substrate 1 are formed. A p-type well~~
~~(hereinafter referred to "p-well") 3 is formed in an upper layer of~~
~~the silicon substrate 1. A p-type low concentration layer 5 is formed~~
~~on an extreme surface layer of a channel portion of the p-well 3.~~
30 ~~Although a detailed description will be given later, this p-type~~
~~low concentration layer 5 is formed using the counter-doping of n-type~~
~~impurities. The p-type low concentration layer 5 has a lower impurity~~
~~concentration than the p-well 3 around this layer 5. By forming the~~

~~p-type low concentration layer 5 in the extreme surface layer of the channel portion, it is possible to perform the control of the threshold voltage of a MISFET with high accuracy (which will be described later). The depth of the p-type low concentration layer 5 is several nanometers to 10 nm or the like from the surface of the silicon substrate 1. At positions deeper than this level, the p-type low concentration layer is offset by the p well 3. A silicon oxide film 6a is formed on the p-type low concentration layer 5. On the silicon oxide film 6a, a HfAlOx film is formed as a high-k gate dielectric layer 7a. The HfAlOx film 7a has a higher dielectric constant than the silicon oxide film 6a.~~ 8 is a diagram for showing a relationship between a threshold voltage and a gate length of a p-type channel MISFET according to various preferred embodiments of the present invention.

15 DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0019]

~~A gate electrode 8a made from a polycrystalline silicon film is formed on the HfAlOx film 7a. Sidewall spacers 13 made from a silicon nitride film are formed on sides of the gate electrode 8a through a silicon oxide film 12. The silicon oxide film 12 is served for damage prevention. In the upper layer of the p well 3 under the sidewall spacers 13, n-type extension regions 11a are formed in such a manner as to sandwich a p-type low concentration layer 5a. In addition, n-type source/drain regions 15a connected to this n-type extension regions 11a are formed in the upper layer of the p well 3.~~

In the following, principles and preferred embodiments of the present invention will be described with reference to the accompanying drawings. The members and steps that are common to some of the drawings are given the same reference numerals and redundant descriptions therefore may be omitted.

First Preferred Embodiment

[0020]

~~Next, Fig. 1 is a method for manufacturing the above-described semiconductor device will be described.~~

~~Figs. 2A to 2F are sectional process views~~view for describing a method for manufacturing a semiconductor device according to the a first preferred embodiment of the present invention. Concretely,
5 ~~Figs. 2A to 2F are~~ More specifically, Fig. 1 is a sectional process view for describing a method for manufacturing a an n-type channel MISFET (hereinafter referred to "NMISFET").

[0021]

10 ~~First, as~~ As shown in Fig. 2A1, element isolation structures 2 each made from for isolating active regions of a silicon oxide film substrate 1 are formed in a p-type silicon substrate 1 by a STI (shallow trench isolation) process. Boron ions as p-type impurities are implanted into active regions isolated by the element isolation
15 ~~structures 2 with a dosage of, for example, 1×10^{13} atoms/cm² and with an acceleration voltage of 130 keV. Thereafter, a heat treatment is performed to form a p-well 3.~~ A p-type well (hereinafter referred to "p-well") 3 is formed in an upper layer of the silicon substrate 1. A p-type low-concentration layer 5 is formed on an extreme surface layer of a channel portion of the p-well 3. Although a detailed description will be given later, this p-type low-concentration layer 5 is preferably formed using the counter-doping of n-type impurities. The p-type low-concentration layer 5 has a lower impurity concentration than the p-well 3 around this layer 5. By forming the p-type
20 low-concentration layer 5 in the extreme surface layer of the channel portion, it is possible to perform the control of the threshold voltage of a MISFET with high accuracy (which will be described later). The depth of the p-type low-concentration layer 5 is several nanometers to 10 nm or the like from the surface of the silicon substrate 1.
25 At positions deeper than this level, the p-type low-concentration layer is offset by the p-well 3. A silicon oxide film 6a is formed on the p-type low-concentration layer 5. On the silicon oxide film 6a, a HfAlOx film is formed as a high-k gate dielectric layer 7a.
30

The HfAlOx film 7a has a higher dielectric constant than the silicon oxide film 6a.

[0022]

5 A gate electrode 8a made from a polycrystalline silicon film
is formed on the HfAlOx film 7a. Sidewall spacers 13 made from a
silicon nitride film are formed on sides of the gate electrode 8a
through a silicon oxide film 12. The silicon oxide film 12 is served
for damage prevention. In the upper layer of the p-well 3 under the
sidewall spacers 13, n-type extension regions 11a are formed in such
10 a manner as to sandwich a p-type low-concentration layer 5a. In
addition, n-type source/drain regions 15a connected to the n-type
extension regions 11a are formed in the upper layer of the p-well
3.

[0023]

15 Next, a method for manufacturing the above-described
semiconductor device will be described.

[0024]

Figs. 2A to 2F are sectional process views for describing a method
for manufacturing a semiconductor device according to the first
20 preferred embodiment of the present invention. More specifically,
Figs. 2A to 2F are sectional process view for describing a method
for manufacturing a NMISFET.

[0025]

First, as shown in Fig. 2A, element isolation structures 2 each
25 made from a silicon oxide film are formed in a p-type silicon substrate
1 by a STI (shallow trench isolation) process. Boron ions as p-type
impurities are implanted into active regions isolated by the element
isolation structures 2 with a dosage of, for example, 1×10^{13} atoms/cm²
and with an acceleration voltage of 130 keV. Thereafter, a heat
30 treatment is performed to form a p-well 3.

[0026]

Next, as shown in Fig. 2B, arsenic ions as n-type impurities
4 are implanted into an extreme surface layer of the p-well 3, i.e.,

an extreme surface layer of a portion to be a channel region of the p-well 3 (hereinafter referred to as a "channel portion") with a dosage of, for example, $5 \text{ to } 8 \times 10^{12} \text{ atoms/cm}^2$ and with an acceleration voltage of 80 keV. Thereafter, a heat treatment is performed with a temperature of 850°C for 30 seconds or so. Thus, the arsenic ions are diffused. As shown in Fig. 2C, a p-type low-concentration layer 5 having a lower impurity concentration than the p-well 3 is formed in the extreme surface layer of the p-well 3. Although a detailed description will be given later, this p-type low-concentration layer 5a makes it possible to control the threshold voltage of the MISFET having a high-k gate dielectric layer 7 with high accuracy.

[00230027]

Next, as shown in Fig. 2C, a silicon oxide film 6 is formed using a thermal oxidation process on the p-type low-concentration layer 5 in a film thickness of, for example, 0.7 nm to 1.0 nm. On the silicon oxide film 6, an HfAlOx film as a high-k gate dielectric layer 7 having a higher dielectric constant than the silicon oxide film 6 is formed in a film thickness of, for example, 1.2 nm to 2.5 nm. Furthermore, a polycrystalline silicon film 8 to be a gate electrode is formed on the HfAlOx film 7 using silane gas as a material in a film thickness of, for example, 125 nm or so. Although not shown, phosphorus ions as gate dopants are implanted into the polycrystalline silicon film 8 with a dosage of, for example, $1 \times 10^{16} \text{ atoms/cm}^2$. Thereafter, the gate dopant implanted in the polycrystalline silicon film 8 is diffused by performing heat treatment. Furthermore, a resist pattern 9 is formed by a lithography technique on the polycrystalline silicon film 8.

[00240028]

Subsequently, the polycrystalline silicon film 8, the HfAlOx film 7 and the silicon oxide film 6 are etched in this order by using the resist pattern 9 as a mask. Thereafter, the resist pattern 9 is removed. Thus, as shown in Fig. 2D, a gate electrode 8a is formed on the p-type low-concentration layer 5 of the silicon substrate 1

through gate dielectric layers 6a, 7a. That is, the p-type low-concentration layer 5 is positioned in an extreme surface layer of a channel region immediately under the gate dielectric layer 6a. Next, arsenic ions 10 as n-type impurities are implanted with an acceleration voltage of 2 keV and with a dosage of, for example, 1×10^{15} atoms/cm² using the gate electrode 8a as a mask, whereby n-type impurity layers 11 are formed. Thereafter, a heat treatment is performed. Thus, the arsenic ions in the n-type impurity layers 11 are activated and, as shown in Fig. 2E, n-type extension regions 11a are formed in the silicon substrate 1.

[00250029]

Next, a silicon oxide film 12 for damage prevention is formed on an entire surface of the substrate 1 in a film thickness of, for example, 2 nm. A silicon nitride film 13 is formed on the silicon oxide film 12 in a film thickness of, for example, 50 nm to 80 nm. Subsequently, the silicon nitride film 13 and the silicon oxide film 12 are anisotropically etched. Thus, as shown in Fig. 2E, sidewall spacers 13 covering sides of the gate electrode 8a are formed in a self-aligning manner. Next, arsenic ions 14 as n-type impurities are implanted, for example, with an acceleration voltage of 35 keV and with a dosage of 5×10^{15} atoms/cm² using the sidewall spacers 13 and the gate electrode 8a as masks, whereby n-type impurity layers 15 are formed. Thereafter, a heat treatment is performed. Thus, the arsenic ions in the n-type impurity layer 15 are activated and, as shown in Fig. 2F, n-type source/drain regions 15a having a higher concentration than the n-type extension region 11 are formed in the silicon substrate 1.

{0026}

~~As described above, in this first embodiment, after the formation of the p-well 3, the arsenic ions 4 are implanted into the extreme surface layer of the channel portion of the p-well 3. Thereafter, a heat treatment is performed. Thus, the p-type low-concentration layer 5 having a lower impurity concentration than the p-well 3 is~~

formed in the extreme surface layer of p well 3. As a result, even in a case where a HfAlO_x film containing metals is used as a gate dielectric layer, it is possible to control the threshold voltage of a MISFET. Therefore, the threshold voltage of a semiconductor having a high k gate dielectric layer can be controlled with high accuracy.

{0027}

Incidentally, in this first embodiment, the description has been given of a n type channel MISFET. However, the present invention can also be applied to a p type channel MISFET. In this case, a n type well (hereinafter referred to "n well") is formed by implanting phosphorus ions with a dosage of 1×10^{13} atoms/cm² and with an acceleration voltage of 300 keV after the formation of the element isolation structures 2 and by performing heat treatment. Thereafter, boron ions as p type impurities are implanted into the extreme surface layer of the channel portion of the n type well with a dosage of, for example, 3 to 5×10^{12} atoms/cm² and with an acceleration voltage of 15 keV, and a heat treatment is performed. Thus, a p type low concentration layer is formed. Then, a MISFET is formed by the same technique as for a PMIS region of the second embodiment, which will be described below.

{0028}

Also, in this first embodiment, the description has been given of a MISFET having a LDD (lightly doped drain) structure. However, the present invention can also be applied to a MISFET having no LDD structure. (the same thing applies also to the second embodiment, which will be described later). In this case, n type impurities for forming n type source/drain regions is implanted into the silicon substrate 1 by using the gate electrode 8a as a mask after the patterning of the gate electrode.

{0029}

Also, it is possible to use a silicon nitride film or a silicon oxynitride film in place of the silicon oxide film 6. Furthermore,

~~it is possible to use a hafnium oxide film (HfO_2 film, hafnia film), a Hf silicate film (HfSiO_x film) or an aluminum oxide film (Al_2O_3 film, alumina film) or films obtained by nitriding these films as the high-k gate dielectric layer 7 in addition to the HfAlO_x film (Hf aluminate film). Also, the high-k gate dielectric layer 7 may be formed directly on the silicon substrate 1 without the formation of the silicon oxide film 6 (the same thing applies also to the second embodiment, which will be described later).~~

[0030]

10 ~~Furthermore, it is possible to use a polycrystalline silicon germanium film in place of a polycrystalline silicon film as the gate electrode material film 8 (the same thing applies also to the second embodiment, which will be described later).~~

As described above, in this first preferred embodiment, after
15 the formation of the p-well 3, the arsenic ions 4 are implanted into the extreme surface layer of the channel portion of the p-well 3. Thereafter, a heat treatment is performed. Thus, the p-type low-concentration layer 5 having a lower impurity concentration than the p-well 3 is formed in the extreme surface layer of p-well 3. As
20 a result, even in a case where an HfAlO_x film containing metals is used as a gate dielectric layer, it is possible to control the threshold voltage of a MISFET. Therefore, the threshold voltage of a semiconductor having a high-k gate dielectric layer can be controlled with high accuracy.

25 [0031]

~~Also, in order to form the p-type low concentration layer 5, it is possible to implant phosphorus ions in place of the arsenic ions 4 with a dosage of, for example, $5 \text{ to } 8 \times 10^{12}$ atoms/ cm^2 and with an acceleration voltage of 35 keV (the same thing applies also to~~
30 ~~the second embodiment, which will be described later). Also in this case, a p-type low concentration layer of the same depth can be obtained.~~

~~Second Embodiment~~

Incidentally, in this first preferred embodiment, the description has been given of a n-type channel MISFET. However, the present invention can also be applied to a p-type channel MISFET. In this case, an n-type well (hereinafter referred to "n-well") is formed by implanting phosphorus ions with a dosage of 1×10^{13} atoms/cm² and with an acceleration voltage of 300 keV after the formation of the element isolation structures 2 and by performing heat treatment. Thereafter, boron ions as p-type impurities are implanted into the extreme surface layer of the channel portion of the n-type well with a dosage of, for example, 3 to 5×10^{12} atoms/cm² and with an acceleration voltage of 15 keV, and a heat treatment is performed. Thus, a p-type low-concentration layer is formed. Then, a MISFET is formed by the same technique as for a PMIS region of the second preferred embodiment, which will be described below.

[0032]

~~Fig. 3 is a sectional view for describing a semiconductor device according to a second embodiment of the present invention. Concretely, Fig. 3 is a sectional view for describing a CMISFET (complementary MISFET) serving as a complementary semiconductor device.~~

Also, in this first preferred embodiment, the description has been given of a MISFET having a LDD (lightly doped drain) structure. However, the present invention can also be applied to a MISFET having no LDD structure. The same thing applies also to the second preferred embodiment, which will be described later. In this case, n-type impurities for forming n-type source/drain regions is implanted into the silicon substrate 1 by using the gate electrode 8a as a mask after the patterning of the gate electrode.

[0033]

~~As shown~~ Also, it is possible to use a silicon nitride film or a silicon oxynitride film in Fig. 3, element isolation structures 22 for isolating active regions of a silicon substrate 21 are formed. A NMIS region and a PMIS region are defined by the element isolation

structures 22. ~~A p well 23 is formed in an upper layer of the silicon substrate 21 of the NMIS region. A n well 24 is formed in an upper layerplace of the silicon substrate 21 of the PMIS region. A p type low concentration layer 27 is formed in an extreme surface layer of a channel portion of the p well 23. A n type low concentration layer 30 is formed in an extreme surface layer of a channel portion of oxide film 6. Furthermore, it is possible to use a hafnium oxide film (HfO_2 film, hafnia film), a Hf silicate film (HfSiOx film) or an aluminum oxide film (Al_2O_3 film, alumina film) or films obtained by nitriding these films as the high-k gate dielectric layer 7 in addition to the HfAlOx film (Hf aluminate film). Also, the n well 24. Although a detailed description will high-k gate dielectric layer 7 may be given later, the p type low concentration layer 27 and formed directly on the silicon substrate 1 without the n type low concentration layer 30 are formed by counter doping n type impurities and p type impurities. The p type and n type low concentration layers 27, 30 have lower impurity concentrations than the p well 23 and n well 24 around formation of the silicon oxide film 6 (the layers 27, 30. By forming same thing applies also to the p type low concentration layer 27 and the n type low concentration layer 30 in the extreme surface layer of the channel portion, it is possible to perform the control of the threshold voltage of a n type channel MISFET and a p type channel MISFET with high accuracy (second embodiment, which will be described later). The depth of the p type low concentration layer 27 and the n type low concentration layer 30 is several nanometers to 10 nm or the like from the surface of the silicon substrate 21. At positions deeper than this level, the p type low concentration layer 27 and the n type low concentration layer 30 are offset by the p well 23 and the n well 24. A silicon oxide film 31a is formed on each of the p type low concentration layer 27 and the n type low concentration layer 30. On the silicon oxide film 31a, a HfAlOx film is formed as a high-k gate dielectric layer 32a. The HfAlOx film 32a has a higher dielectric constant than the silicon oxide film 31a.~~

[0034]

~~A gate electrode 33a made from~~ Furthermore, it is possible to use a polycrystalline silicon germanium film ~~is formed on~~ in place of a polycrystalline silicon film as the ~~HfAlO_x film 32a~~. Sidewall spacers 42 made from a silicon nitride gate electrode material film are formed on sides of 8 (the gate electrode 33a through a silicon oxide film 41. The silicon oxide film 41 is served for damage prevention same thing applies also to the second preferred embodiment, which will be described later).

10 [0035]

~~In the upper layer of the p well 23 under the sidewall spacers 42 in the NMIS region, n-type extension regions 37a are formed in such a manner as to sandwich the p-type low concentration layer 27. In addition, n-type source/drain regions 45a connected to the n-type extension regions 37a are formed in the upper layer of the p well 23.~~

Also, in order to form the p-type low-concentration layer 5, it is possible to implant phosphorus ions in place of the arsenic ions 4 with a dosage of, for example, $5 \text{ to } 8 \times 10^{12} \text{ atoms/cm}^2$ and with an acceleration voltage of 35 keV (the same thing applies also to the second embodiment, which will be described later). Also in this case, a p-type low-concentration layer of the same depth can be obtained.

25 Second Preferred Embodiment

[0036]

~~Also, in the upper layer of the n well 24 under the sidewall spacers 42 in the PMIS region, p-type extension regions 40a are formed in such a manner as to sandwich the n-type low concentration layer 30. In addition, p-type source/drain regions 48a connected to the n-type extension regions 40a are formed in the upper layer of the n well 24.~~

Fig. 3 is a sectional view for describing a semiconductor device according to a second preferred embodiment of the present invention. Concretely, Fig. 3 is a sectional view for describing a CMISFET (complementary MISFET) serving as a complementary semiconductor device.

[0037]

~~Next, a method for manufacturing the above-described semiconductor device will be described.~~

~~Figs. 4A to 6C are sectional process views for describing a method for manufacturing a semiconductor device according to the second embodiment of the present invention. Concretely, these figures are sectional process views for describing a method for manufacturing a CMISFET serving as a complementary semiconductor device.~~

As shown in Fig. 3, element isolation structures 22 for isolating active regions of a silicon substrate 21 are formed. A NMIS region and a PMIS region are defined by the element isolation structures 22. A p-well 23 is formed in an upper layer of the silicon substrate 21 of the NMIS region. An n-well 24 is formed in an upper layer of the silicon substrate 21 of the PMIS region. A p-type low-concentration layer 27 is formed in an extreme surface layer of a channel portion of the p-well 23. An n-type low-concentration layer 30 is formed in an extreme surface layer of a channel portion of the n-well 24. Although a detailed description will be given later, the p-type low-concentration layer 27 and the n-type low-concentration layer 30 are formed by counter-doping n-type impurities and p-type impurities. The p-type and n-type low-concentration layers 27, 30 have lower impurity concentrations than the p-well 23 and n-well 24 around the layers 27, 30. By forming the p-type low-concentration layer 27 and the n-type low-concentration layer 30 in the extreme surface layer of the channel portion, it is possible to perform the control of the threshold voltage of an n-type channel MISFET and a p-type channel MISFET with high accuracy (which will be described later). The depth of the p-type low-concentration layer 27 and the

n-type low-concentration layer 30 is several nanometers to 10 nm or the like from the surface of the silicon substrate 21. At positions deeper than this level, the p-type low-concentration layer 27 and the n-type low-concentration layer 30 are offset by the p-well 23 and the n-well 24. A silicon oxide film 31a is formed on each of the p-type low-concentration layer 27 and the n-type low-concentration layer 30. On the silicon oxide film 31a, a HfAlOx film is formed as a high-k gate dielectric layer 32a. The HfAlOx film 32a has a higher dielectric constant than the silicon oxide film 31a.

10 [0038]

First, as shown in Fig. 4A, element isolation structures 22 are formed in a p-type silicon substrate 21 by the STI process. Next, boron ions as p-type impurities are implanted into active regions of a n-type channel MISFET region (hereinafter referred to as "NMIS region") isolated by the element isolation structures 22 with a dosage of, for example, 1×10^{13} atoms/cm² and with an acceleration voltage of 130 keV. Thereafter, a heat treatment is performed to diffuse the boron ions. Thus, a p-well 23 is formed.

Also, phosphorus ions as n-type impurities are implanted into active regions of a p-type channel MISFET region (hereinafter referred to as "PMIS region") with a dosage of, for example, 1×10^{13} atoms/cm² and with an acceleration voltage of 300 keV. Thereafter, a heat treatment is performed to diffuse the phosphorus ions. Thus, n-well 24 is formed. Incidentally, the p-type impurities and the n-type impurities can be diffused by performing heat treatment once.

A gate electrode 33a made from a polycrystalline silicon film is formed on the HfAlOx film 32a. Sidewall spacers 42 made from a silicon nitride film are formed on sides of the gate electrode 33a through a silicon oxide film 41. The silicon oxide film 41 is provided for damage prevention.

30 [0039]

Next, as shown in Fig. 4B, a resist pattern 25 covering the PMIS region is formed using a lithography technique. Arsenic ions as n-type

impurities 26 are implanted into an extreme surface layer of the p-well 23, i.e., an extreme surface layer of a channel portion of the p-well 23 with a dosage of, for example, $5 \text{ to } 8 \times 10^{12} \text{ atoms/cm}^2$ and with an acceleration voltage of 80 keV. Thereafter, the resist pattern 25 is removed.

In the upper layer of the p-well 23 under the sidewall spacers 42 in the NMIS region, n-type extension regions 37a are formed so as to sandwich the p-type low-concentration layer 27. In addition, n-type source/drain regions 45a connected to the n-type extension regions 37a are formed in the upper layer of the p-well 23.

[0040]

Next, as shown Also, in Fig. 4C, a resist pattern 28 covering the NMIS upper layer of the n-well 24 under the sidewall spacers 42 in the PMIS region is, p-type extension regions 40a are formed using a lithography technique. Boron ions as p-type impurities 29 are implanted into an extreme surface layer of the n-well 24, i.e., an extreme surface layer of a channel portion of so as to sandwich the n-well 24 with a dosage of, for example, $3 \text{ to } 5 \times 10^{12} \text{ atoms/cm}^2$ and with an acceleration voltage of 15 keV. The resist pattern 28 is removed.

Thereafter, a heat treatment is performed with a temperature of 850°C for about type low-concentration layer 30 seconds or so. Thus, as shown in Fig. 5A, p-type low concentration layers 27 are formed in the extreme surface layer of the p-well 23, and n-type low concentration layers 30 are formed in the extreme surface. In addition, p-type source/drain regions 48a connected to the n-type extension regions 40a are formed in the upper layer of the n-well 24.

[0041]

Next, as shown in Fig. 5A, a silicon oxide film 31 is formed using method for manufacturing the thermal oxidation process on the silicon substrate 21 in a film thickness of, for example, 0.7 nm to 1.0 nm. On the silicon oxide film 31, a HfAlOx film is formed as

a high-k gate dielectric layer 32 in a film thickness of, for example, 1.2 nm to 2.5 nm. The HfAlOx film 32 has a higher dielectric constant than the silicon oxide film 31. Furthermore, a polycrystalline silicon film 33 to above-described semiconductor device will be a gate
5 electrode is formed on the HfAlOx film 32 using silane gas as a material
in a film thickness of, for example, 125 nm or so described.

[0042]

Although not shown, the PMIS region is masked with a resist pattern, and phosphorus ions as gate dopants are implanted into the
10 polycrystalline silicon film 33 of the NMIS region with a dosage of,
for example, 1×10^{16} atoms/cm². By using a similar technique, the NMIS region is masked with a resist pattern, and boron ions as gate dopants are implanted into the polycrystalline silicon film 33 of the PMIS region with a dosage of, for example, 3×10^{15} atoms/cm².
15 The gate dopants implanted in the polycrystalline silicon film 33
are diffused by performing a heat treatment.

Figs. 4A to 6C are sectional process views for describing a method
for manufacturing a semiconductor device according to the second
preferred embodiment of the present invention. More specifically,
20 these figures are sectional process views for describing a method
for manufacturing a CMISFET serving as a complementary semiconductor
device.

[0043]

Next, a resist pattern 34 is formed on the polycrystalline silicon
25 film 33 using the lithography technique. First, as shown in Fig. 4A,
element isolation structures 22 are formed in a p-type silicon
substrate 21 by the STI process. Next, boron ions as p-type impurities
are implanted into active regions of a n-type channel MISFET region
(hereinafter referred to as "NMIS region") isolated by the element
30 isolation structures 22 with a dosage of, for example, 1×10^{13} atoms/cm²
and with an acceleration voltage of 130 keV. Thereafter, a heat
treatment is performed to diffuse the boron ions. Thus, a p-well
23 is formed.

[0044]

The polycrystalline silicon film 33, the HfAlO_x film 32 and the silicon oxide film 31 are etched in this order using the resist pattern 34 as a mask. Next, the resist pattern 34 is removed. Thus, as shown in Fig. 5B, a gate electrode 33a is formed on the n-type low concentration layer 27 of the NMIS region through gate dielectric layers 31a, 32a, and a gate electrode 33a is formed on the p-type low concentration layer 30 of the PMIS region through gate dielectric layers 25a, 26a.

Also, phosphorus ions as n-type impurities are implanted into active regions of a p-type channel MISFET region (hereinafter referred to as "PMIS region") with a dosage of, for example, 1×10^{13} atoms/cm² and with an acceleration voltage of 300 keV. Thereafter, a heat treatment is performed to diffuse the phosphorus ions. Thus, the n-well 24 is formed. Incidentally, the p-type impurities and the n-type impurities can be diffused by performing heat treatment once.

[0045]

Next, as shown in Fig. 5B4B, a resist pattern 3525 covering the PMIS region is formed using a lithography technique. Arsenic ions 36 as n-type impurities for forming n-type extension regions 26 are implanted with into an acceleration voltage of 2 keV and with a dosage of, for example, 1×10^{15} atoms/cm² using extreme surface layer of the gate electrode 33a of the NMIS region as a mask. Thus, n-type impurity layers 37 are formed in p-well 23, i.e., an extreme surface layer of a channel portion of the p-well 23 with a dosage of, for example, 5 to 8×10^{12} atoms/cm² and with an acceleration voltage of 80 keV. Thereafter, the silicon substrate 21 of the NMIS region. The resist pattern 3525 is removed.

[0046]

Next, as shown in Fig. 5C4C, a resist pattern 3828 covering the NMIS region is formed using a lithography technique. Boron ions 39 as p-type impurities for forming p-type extension regions 29 are implanted with into an acceleration voltage of 0.2 keV and with a dosage

of, for example, 1×10^{15} atoms/cm² using the gate electrode 33a of the PMIS region as a mask. Thus, a p-type impurity layer 40 is formed on the silicon substrate 21 of the PMIS region extreme surface layer of the n-well 24, i.e., an extreme surface layer of a channel portion of the n-well 24 with a dosage of, for example, 3 to 5×10^{12} atoms/cm² and with an acceleration voltage of 15 keV. The resist pattern 28 is removed.

Thereafter, a heat treatment is performed. Thus, as shown in Fig. 6A, the arsenic ions in the n-type impurity layer 37 of the NMIS region are activated to form n-type extension regions 37a, and the boron ions in the p-type impurity layer 40 of the PMIS region are activated to form p-type extension regions 40a.

[0047]

Next, as shown in Fig. 6A, a silicon oxide film 41 is formed on the entire surface of the substrate 21 in a film thickness of, for example, 2 nm. A silicon nitride film 42 is formed on the silicon oxide film 41 in a film thickness of, for example, 50 nm to 80 nm. Subsequently, the silicon nitride film 42 and the silicon oxide film 41 are anisotropically etched. Thus, sidewall spacers 42 covering sides of the gate electrode 33a are formed in a self-aligning manner.

Thereafter, a heat treatment is performed with a temperature of 850°C for about 30 seconds or so. Thus, as shown in Fig. 5A, p-type low-concentration layers 27 are formed in the extreme surface layer of the p-well 23, and n-type low-concentration layers 30 are formed in the extreme surface layer of the n-well 24.

[0048]

Next, a resist pattern 43 covering the PMIS region is formed using a lithography technique. Arsenic ions 44 as n-type impurities for forming n-type source/drain regions are implanted with an acceleration voltage of 35 keV and with a dosage of, for example, 5×10^{15} atoms/cm² using the sidewall spacers 42 and the gate electrode 33a of the NMIS region as masks. Thus, n-type impurity layers 45

are formed in the upper layer of the silicon substrate 21 of the NMIS region. The resist pattern 43 is removed.

Next, as shown in Fig. 5A, a silicon oxide film 31 is formed using the thermal oxidation process on the silicon substrate 21 in a film thickness of, for example, 0.7 nm to 1.0 nm. On the silicon oxide film 31, an HfAlOx film is formed as a high-k gate dielectric layer 32 in a film thickness of, for example, 1.2 nm to 2.5 nm. The HfAlOx film 32 has a higher dielectric constant than the silicon oxide film 31. Furthermore, a polycrystalline silicon film 33 to be a gate electrode is formed on the HfAlOx film 32 using silane gas as a material in a film thickness of, for example, 125 nm or so.

[0049]

Next, as ~~Although not shown in Fig. 6B,~~ the PMIS region is masked with a resist pattern 46 covering the NMIS region by a lithographic technique. Boron, and phosphorus ions 47 as p-type impurities for forming gate dopants are implanted into the p-type source/drain regions are implanted with an acceleration voltage polycrystalline silicon film 33 of 5 keV and with a dosage of, for example, 3×10^{15} atoms/cm² using the sidewall spacers 42 and the gate electrode 33a of the PMIS region as masks. Thus, p-type impurity layers 48 are formed in the upper layer of the silicon substrate 21 of the PMIS region. The resist pattern 46 is removed. the NMIS region with a dosage of, for example, 1×10^{16} atoms/cm². By using a similar technique, the NMIS region is masked with a resist pattern, and boron ions as gate dopants are implanted into the polycrystalline silicon film 33 of the PMIS region with a dosage of, for example, 3×10^{15} atoms/cm². The gate dopants implanted in the polycrystalline silicon film 33 are diffused by performing a heat treatment.

[0050]

Lastly, as shown in Fig. 6C, a heat treatment is performed with a temperature of not less than 1000°C but not more than 1050°C for several minutes. Thus, the arsenic ions in the n-type impurity layers 45 of the NMIS region are activated to form n-type source/drain regions

45a, and the boron ions in the p-type impurity layers 48 of the PMIS region are activated to form of p-type source/drain regions 48a.

Next, a resist pattern 34 is formed on the polycrystalline silicon film 33 using the lithography technique.

5

[0051]

As described above, in this second embodiment, after the formation of the p-well 23 in the NMIS region and the formation of the n-well 24 in the PMIS region, the arsenic ions 26 are implanted into the extreme surface layer of the channel portion of the p-well 23, and a heat treatment is performed. The polycrystalline silicon film 33, the HfAlOx film 32 and the silicon oxide film 31 are etched in this order using the resist pattern 34 as a mask. Next, the resist pattern 34 is removed. Thus, the p-type low concentration layer 27 having a higher impurity concentration than the p-well 23 is formed. Further, the boron ions 29 are implanted into the extreme surface layer of the channel portion of the n-well 24, and a heat treatment is performed. Thus, the n-type low concentration layer 30 having a lower impurity concentration than the n-well 24 is formed. As a result, even in a case where a HfAlOx film containing metals is used as a gate dielectric layer, it is possible to control the threshold voltage of the n-type channel MISFET and the p-type channel MISFET. Therefore, the threshold voltage of a complementary semiconductor device having a high-k gate dielectric layer can be controlled with high accuracy. as shown in Fig. 5B, a gate electrode 33a is formed on the n-type low-concentration layer 27 of the NMIS region through gate dielectric layers 31a, 32a, and a gate electrode 33a is formed on the p-type low-concentration layer 30 of the PMIS region through gate dielectric layers 25a, 26a.

[0052]

Next, as shown in Fig. 7 is a diagram for showing a relationship between a threshold voltage and a gate length of a n-type channel

MISFET according to the present invention 5B, a resist pattern 35 covering the PMIS region is formed using a lithography technique. Arsenic ions 36 as n-type impurities for forming n-type extension regions are implanted with an acceleration voltage of 2 keV and with a dosage of, for example, 1×10^{15} atoms/cm² using the gate electrode 33a of the NMIS region as a mask. Thus, n-type impurity layers 37 are formed in the silicon substrate 21 of the NMIS region. The resist pattern 35 is removed.

[0053]

10 As Next, as shown in Fig. 7, an increase in the threshold voltage of a NMISFET is observed when ion implantation for impurity concentration control into a channel portion is not performed. The threshold voltage can be suppressed by performing ion implantation. In order to control the threshold voltage of a NMISFET to a preferred range of, concretely, 300 mV to 600 mV with a gate length of not less than 90 nm, which is a minimum value at the present stage, it is preferred that arsenic ions are implanted with a dosage of 5 to 8×10^{12} atoms/cm². In this case, the p well is formed by implanting boron ions with a dosage of 1×10^{13} atoms/cm² and with an acceleration voltage of 130 keV. 5C, a resist pattern 38 covering the NMIS region is formed using a lithography technique. Boron ions 39 as p-type impurities for forming p-type extension regions are implanted with an acceleration voltage of 0.2 keV and with a dosage of, for example, 1×10^{15} atoms/cm² using the gate electrode 33a of the PMIS region as a mask. Thus, a p-type impurity layer 40 is formed on the silicon substrate 21 of the PMIS region.

[0054]

Fig. 8 is a diagram for showing a relationship between a threshold voltage and a gate length of a p-type channel MISFET according to the present invention.

Thereafter, a heat treatment is performed. Thus, as shown in Fig. 6A, the arsenic ions in the n-type impurity layer 37 of the NMIS region are activated to form n-type extension regions 37a, and the

boron ions in the p-type impurity layer 40 of the PMIS region are activated to form p-type extension regions 40a.

5 [0055]

~~As Next, as shown in Fig. 8, as with the above-described NMISFET, an increase in the threshold voltage of a PMISFET is observed when ion implantation for impurity concentration control into a channel portion is not performed. The threshold voltage can be suppressed~~
10 ~~by performing ion implantation. In order to control the threshold voltage of a NFET to a preferred range of, concretely, 400 mV to 600 mV with a gate length of not less than 90 nm, which is a minimum value at the present stage, it is preferred that boron ions are implanted with a dosage of 3 to 5×10^{12} atoms/cm². In this case, the n well~~
15 ~~is formed by implanting phosphorus ions with a dosage of 1×10^{13} atoms/cm² and with an acceleration voltage of 300 keV. 6A, a silicon oxide film 41 is formed on the entire surface of the substrate 21 in a film thickness of, for example, 2 nm. A silicon nitride film 42 is formed on the silicon oxide film 41 in a film thickness of, for example, 50 nm to~~
20 ~~80 nm. Subsequently, the silicon nitride film 42 and the silicon oxide film 41 are anisotropically etched. Thus, sidewall spacers 42 covering sides of the gate electrode 33a are formed in a self-aligning manner.~~

25 **~~Industrial applicability~~**

[0056]

~~As described above, in accordance with the semiconductor device and the method for manufacturing the same of the present invention, by forming a low concentration layer having a low impurity~~
30 ~~concentration in an extreme surface layer of a channel portion of a well region, it is possible to control the threshold voltage of a semiconductor device having a high k gate dielectric layer with high accuracy.~~